

AMENDED CLAIM SET:

1 1. (currently amended) A field effect device, comprising:

2 a crystalline Si body of one conductivity type;

3 a SiGe layer epitaxially disposed on said Si body;

4 a Si layer epitaxially disposed on said SiGe layer; and

5 a source and a drain comprising SiGe in an epitaxial relation with said Si body

6 and connected to each other by said SiGe layer and said Si layer, wherein said source and

7 said drain are formed in recessed source/drain regions of said body, said source and said

8 drain having a conductivity type opposite to that of said Si body and each forming a

9 heterojunction and a metallurgical junction with said Si body, wherein said heterojunction

10 coincides with said metallurgical junction with a tolerance of less than about 10nm.

1 2. (original) The device of claim 1, wherein said tolerance is less than about 5nm.

1 3. (original) The device of claim 1, wherein said Si body is disposed on top of an  
2 insulating layer.

1 4. (original) The device of claim 3, wherein said insulating layer is SiO<sub>2</sub>.

1 5. (original) The device of claim 1, wherein said Si body conductivity is n-type, and  
2 wherein a hole device current is confined predominantly in said SiGe layer.

1 6. (original) The device of claim 5, wherein said hole device current is directed along one  
2 of a <100> or a <110> crystallographic direction.

1 7. (original) The device of claim 1, wherein said Si body conductivity is p-type, and an  
2 electron device current is confined predominantly in said Si layer.

1 8. (original) The device of claim 1, wherein said SiGe layer and said SiGe in said source  
2 and said drain are compressively strained.

1 9. (original) The device of claim 1, wherein said SiGe layer is between about 5nm and  
2 15nm thick.

1 10. (original) The device of claim 1, wherein said SiGe layer has a Ge concentration  
2 which substantially equals a Ge concentration in said SiGe in said source and said drain.

1 11. (original) The device of claim 10, wherein said Ge concentration in said SiGe layer is  
2 between about 15% and 50%.

1 12. (canceled)

1 13. (original) The device of claim 1, wherein said device has a top surface plane that lies  
2 essentially in one of a (100), (110) or (111) crystallographic plane.

1 14. (original) The device of claim 1, wherein said source and said drain further comprise  
2 an epitaxial Si cap layer disposed on top of said strained SiGe, wherein said Si cap layer  
3 is between about 2nm and 30nm thick.

1 15. (currently amended) The device of claim 1, wherein said Si body conductivity is n-  
2 type, and said device is connected in a complementary circuit configuration with a field  
3 effect device comprising:

4 a crystalline Si body of p-type conductivity;

5 a SiGe layer epitaxially disposed on said p-type Si body;

6 a Si layer epitaxially disposed on said SiGe layer; and

7 a source and a drain of n-type conductivity comprising SiGe in an epitaxial  
8 relation with said p-type Si body and connected to each other by said SiGe layer and said  
9 Si layer, wherein said n-type source and said n-type drain are formed in recessed  
10 source/drain regions of said p-type body, said source and said drain each forming a  
11 heterojunction and a metallurgical junction with said p-type Si body, wherein said  
12 heterojunction coincides with said metallurgical junction with a tolerance of less than

1 about 10nm.

1 16. (original) The device of claim 1, wherein said Si body conductivity is n-type, and said  
2 device is connected in a complementary circuit configuration with a field effect device  
3 comprising:

4 a crystalline Si body of p-type conductivity;  
5 a SiGe layer epitaxially disposed on said p-type Si body;  
6 a Si layer epitaxially disposed on said SiGe layer; and  
7 a source and a drain of n-type conductivity comprising SiGe in an epitaxial  
8 relation with said p-type Si body and connected to each other by said SiGe layer and said  
9 Si layer.

1 17. (original) The device of claim 1, wherein said Si body conductivity is n-type, and said  
2 device is connected in a complementary circuit configuration with a field effect device  
3 comprising:

4 a crystalline Si body of p-type conductivity;  
5 a SiGe layer epitaxially disposed on said p-type Si body;  
6 a Si layer epitaxially disposed on said SiGe layer; and  
7 a source and a drain of n-type conductivity connected to each other by said SiGe  
8 layer and said Si layer.

1 18. (original) The device of claim 1, wherein said Si body conductivity is n-type, and said  
2 device is connected in a complementary circuit configuration with an NMOS device.

1 19. (currently amended) A PMOS field effect device, comprising:  
2 a crystalline Si body of n-type conductivity;  
3 a SiGe layer epitaxially disposed on said n-type Si body;  
4 a Si layer epitaxially disposed on said SiGe layer; and  
5 a source and a drain of p-type conductivity comprising SiGe in an epitaxial  
6 relation with said n-type Si body and connected to each other by said SiGe layer and said  
7 Si layer, wherein said p-type source and said p-type drain are formed in recessed  
8 source/drain regions of said n-type body, said source and said drain each forming a  
9 heterojunction and a metallurgical junction with said n-type Si body, wherein said  
10 heterojunction coincides with said metallurgical junction with a tolerance of less than  
11 about 10nm.

1 20. (original) The device of claim 19, wherein said tolerance is less than about 5nm.

1 21. (original) The device of claim 19, wherein said Si body is disposed on top of an  
2 insulating layer.

1 22. (original) The device of claim 21, wherein said insulating layer is SiO<sub>2</sub>.

1 23. (original) The device of claim 19, wherein said SiGe layer is between about 5nm and  
2 15nm thick.

1 24. (original) The device of claim 19, wherein said SiGe layer has a Ge concentration of  
2 between about 15% and 50%.

1 25. (original) The device of claim 24, wherein said Ge concentration in SiGe layer  
2 substantially equals a Ge concentration in said SiGe in said source and said drain.

1 26. - 37. (canceled)

1 38. (currently amended) A processor, comprising:  
2 at least one chip, wherein said chip comprises at least one field effect device, and  
3 wherein said at least one field effect device comprise:  
1 a crystalline Si body of one conductivity type;  
2 a SiGe layer epitaxially disposed on said Si body;  
3 a Si layer epitaxially disposed on said SiGe layer; and  
4 a source and a drain comprising SiGe in an epitaxial relation with said Si body  
5 and connected to each other by said SiGe layer and said Si layer, wherein said source and  
6 said drain are formed in recessed source/drain regions of said body, said source and said  
7 drain having a conductivity type opposite to that of said Si body and each forming a

1 heterojunction and a metallurgical junction with said Si body, wherein said heterojunction  
2 coincides with said metallurgical junction with a tolerance of less than about 10nm.

1 39. (new) A field effect device, comprising:

2 a crystalline Si body of one conductivity type;

3 a SiGe layer epitaxially disposed on said Si body;

4 a Si layer epitaxially disposed on said SiGe layer; and

1 a source and a drain comprising SiGe in an epitaxial relation with said Si body  
2 and connected to each other by said SiGe layer and said Si layer, said source and said  
3 drain having a conductivity type opposite to that of said Si body and each forming a  
4 heterojunction and a metallurgical junction with said Si body, wherein said heterojunction  
5 coincides with said metallurgical junction with a tolerance of less than about 10nm, and  
6 wherein a gate dielectric of said device defines a top surface plane for said device, and  
7 wherein said source and said drain are protruding out of said top surface plane.